REMARKS/ARGUMENTS

Regarding amendments to the claims:

Tabs have been underlined to be added as an amendment. No new matter has been added with respect to the changes made from the last amendment.

Regarding rejections under 35 U.S.C. 103:

Examiner:

1. **Claims 1, 4-7, 9, 11-12 are rejected under 35 U.S.C 103(a) as being anticipated by Steffan et al. (US Pat. 6512842 B1).**

Steffan et al. teaches a method and apparatus for the analysis of defects in semiconductor wafers. In doing so, a production lot of wafers are scanned and analyzed in an analysis tool, such as the SEM (scanning electron microscope), optical tools, or the FIB (fixed ion beam). The analyzed data is then stored in the defect management system, along with images of the wafers and assigned descriptors. Furthermore, a review station is present to assign refined descriptive labels to the images and this data is saved in the database. In addition to the defect inspection process, the ADC (automatic defect classification) protocol is used for classifying the types of defects. As per the limitations of the instant claims, a manual inspection is also taught by the prior art of record. Evidently, an operator is able to review the images at the review station and compare those reviewed to other images in the database. Upon having reviewed the retrieved images, the operator can revise the descriptors to refine the database.

Response:

In contrast to Steffan et al's invention, the claimed invention primarily utilizes a **different generation** approach to first provide a wafer with defects generated from a first

semiconductor process and then utilizes a predetermined defect database with recipe corresponding to a second semiconductor process to verify the defects, in which the second semiconductor process is the previous generation process of the first semiconductor process.

Preferably, if the first semiconductor process were to be an etching process of the 0.13 μm process, the second semiconductor process can be the same etching process from the previous generation, such as an etching process of the 0.15 μm process. By utilizing a recipe generated from the previous generation to verify the defects generated from the newer generation, the claimed invention is able to not only obtain a much higher initial accuracy of classification, but also greatly reduce the classification time as the recipe created by utilizing the second semiconductor process (hence the previous generation) may already include similar design rules, patterns, and defect types as the first semiconductor process (hence the newer generation). As a result, much fewer samples are required to be collected and much less time is needed to complete a defect database.

Despite the fact that Steffan et al discloses a similar method of analyzing defects, such as utilizing descriptors to link to images of various defects and storing the images, descriptors, and linked data in a database, Steffan et al never suggests a method of first providing a wafer with defects generated from a first semiconductor process and utilizing a predetermined defect database with recipe corresponding to a second semiconductor process to verify the defects of the wafer from the first semiconductor process, in which the second semiconductor process is a previous generation process corresponding to the first semiconductor process.

Since the method taught by Steffan et al. is significantly different from the claimed invention, claims 1, 4-7, 9, 11-12 should be allowed. Reconsideration of the rejection of claims 1, 4-7, 9, 11-12 is respectively requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

Winston Hsu Date: Oct. 19, 2005

Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)